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A33890-066340.0126

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TO ALL WHOM IT MAY CONCERN:

Be it known that WE, MATTHIAS WEISS and GERHARD FETTWEIS, citizens of Germany, residing in Dresden, Germany whose post office addresses are Bernhardstraße 111, 01187 Dresden, Germany; and Plattleite 39, 01324 Dresden, Germany, respectively, have invented an improvement in

METHOD AND APPARATUS FOR PRODUCING INSTRUCTION WORDS
TO TRIGGER FUNCTIONAL UNITS IN A PROCESSOR

of which the following is a

SUBSTITUTE SPECIFICATION

BACKGROUND OF THE INVENTION

[0001] The invention relates to a method of generating instruction words to trigger functional units in a processor, where, in a configuration phase, a sequence of primary instruction words deriving from a translation of a program code is generated, each primary instruction word consisting of several instruction word parts and each instruction word part is intended to trigger a functional unit of the processor, and the instruction word part in one or several primary instruction words serves to execute a data-stationary command. In a known arrangement each primary instruction word may

be compressed and provided as a program word in an execution memory. In an execution phase, secondary instruction words corresponding to the primary instruction words are synthesized out of the stored program words.

[0002] The invention relates further to an apparatus for producing instruction words to trigger functional units in a processor having functional units, having an instruction word memory associated with said functional units, and having an instruction word buffer for storing instruction words already generated with a latitude at least equal to the bit latitude of the secondary instruction word, the instruction word buffer consisting of a memory having alternative or fixedly programmed line access.

[0003] In German Patent DE 198 59 389 C1, a method and an apparatus for triggering functional units in a processor are described. By this method and the associated apparatus, while retaining a small program word latitude, the working speed is application-specifically enhanced.

[0004] The inventors have realized that further enhancement in working speed is possible because some of the commands are data-stationary. Data-stationary means, in this case, that a command affords no definite information on the route by which a processor is to execute the command, in particular the number of steps required to carry out the command.

[0005] In the execution of a data-stationary command, various steps are carried out in several beats. Each of these steps is carried out by an instruction word part in one instruction word of a sequence of instruction words, each instruction word part prompting

a functional unit of the processor to perform a certain action carrying out a partial step of the execution of the command.

[0006] Each instruction word, according to the known approach, must be newly composed over the sequence of program words. Even in the case of performing identical commands, it is necessary to generate instruction words corresponding to the partial steps of each command and to compose the program words for this purpose. This is necessary also in the case of identical commands, that is, for like command sequences, new, albeit identical program word sequences are required again and again. This entails a large memory utilization and considerable processing time.

[0007] It is an object of the invention, then, to reduce the memory utilization and enhance the working speed.

SUMMARY OF THE INVENTION

[0008] The invention makes it possible to describe the processing of the commands of most frequent occurrence, always performed with the same hardware components and always on the same routes, with the corresponding instruction word parts stored in a complex word sequence. When such a command occurs, the contents of the complex word tables may be consulted to retrieve the instruction word parts for command execution. The special treatment of each recurring command as a normal (variable) command may be eliminated, thereby relieving the program word memory and enhancing the working speed.

[0009] The invention will be illustrated below in more detail with reference to an embodiment by way of example.

BRIEF DESCRIPTION OF THE DRAWING

[0010] The drawing shows an embodiment of complex word processing according to the invention.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENT

[0011] In the method of triggering functional units 12 in a processor 13 as represented in the figure of the drawing, in accordance with the prior art and hence according to German Patent DE 198 59 389 C1, from a program code 1 by means of a translation in a configuration phase, a sequence of primary instruction words 2 consisting of several instruction word parts 4 is generated. Further, the sequence of primary instruction words 2 is compressed in the program word production 8 and stored as a sequence of corresponding program words in an execution memory 9.

[0012] According to a preferred arrangement according to the invention, within the configuration phase, the instruction word parts 4 serving to execute a data-stationary command are assembled in a complex word sequence 18 and stored in a line, indicated by the complex word pointer 6, of the complex word table stored in complex word memory 5. The complex word pointers 6 are themselves stored in the execution memory 9.

[0013] In an execution phase, complex word pointers 6, occurring in the execution memory 9, are recognized and, with the index they contain, specify the line of the complex word table 5 to be read out, which contains the associated complex word sequence 18.

[0014] The complex word sequence 18 is read out, and the complex words 17 contained in it are transferred in parallel to the corresponding rows and columns of the secondary instruction word memory 7 following assignments internal to the complex words. The complex word table may generated during the configuration phase of processing or may be a fixed table of complex words that we called by specified pointers corresponding to program commands.

[0015] Corresponding to the adjusted secondary instruction word memory sequence 16, firstly the current secondary instruction word 15 is transferred into an instruction word output memory 11. Its output triggers the functions required for processing at the corresponding functional units 12 of the processor 13.

[0016] The current secondary instruction word 15 is also processed in a secondary instruction word production 10 unit together with a new program word, so that at its output, an additional secondary instruction word 15 is placed in readiness for storage in the secondary instruction word memory 7.